REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application. Further, Applicant thanks the Examiner for the courtesies extended in the telephonic Examiner Interview of November 4, 2004.

Disposition of Claims

Claims 1-6 and 8-17 are pending in the present application. Claims 1 and 8 are independent. The remaining claims depend, directly or indirectly, from claims 1 and 8.

Rejection(s) under 35 U.S.C § 103

Claims 1, 2, 3, 5, 8, and 17

Claims 1, 2, 3, 5, 8, and 17 were rejected under 35 U.S.C. § 103 as being unpatentable over Applicant's Prior Art ("APA") in view of United Kingdom Patent No. 2098001A issued to Schaper (hereinafter "Schaper"). For the reasons set forth below, this rejection is respectfully traversed.

The present invention is directed to a "flip-chip" semiconductor package assembly having a semiconductor die and a capacitor having an aperture in the central portion of the capacitor. The semiconductor die has an active side that faces a portion of a top surface of the package substrate. Additionally, power connections are located between the active side and the package substrate. Power is distributed to and from the semiconductor die in this manner. A flip-chip semiconductor has an active side of the semiconductor die facing the substrate.

As discussed with reference to Figure 4 of the present application, one exemplary

embodiment of the present invention comprises a windowframe capacitor (27) that surrounds semiconductor die (11). As shown in Figure 5 of the present application, power connections (14) are positioned between an active side of the semiconductor die (11) and the package substrate (13).

Accordingly, independent claim 1 requires the combination of (i) a unitary capacitor having an aperture arranged to surround a semiconductor die and a bottom surface provided with electrical power connections adapted to be connected to a substrate, and (ii) a semiconductor die having an active side adapted to face and be connected to the substrate, where the active side has power connections arranged to distribute power to and from the semiconductor die. Independent claim 8 requires (i) a semiconductor die having an active side that faces a portion of the top surface of the package substrate, where the power connections between the active side and the package substrate distribute power to and from the semiconductor die, and (ii) a unitary windowframe capacitor having an aperture formed therein and mounted on the top surface of the package substrate surrounding the semiconductor die.

As seen with reference to Figure 1 of the present application, Applicant's Prior Art teaches the use of a flip-chip package that is mounted with an active side of a semiconductor die **11** facing a package substrate **13**. Applicant's Prior Art additionally teaches the use of individual capacitors on top of the package substrate **13** (see, *e.g.*, paragraph [0003] of the present application). However, Applicant's Prior Art does not teach a unitary windowframe capacitor, provided on the surface **12** of the semiconductor die, as seen with reference to Figure 4 of the present application. A windowframe capacitor allows for a greater utilization of the surface area of the package substrate **13**.

Additionally, as opposed to using individual high-frequency capacitors, the effective capacitance may be increased while the inductance may be decreased. Further, the top area of the windowframe capacitor remains available for mounting other electronic components (see, *e.g.*, paragraph [0023] of the present application).

In contrast to the present invention, Schaper contemplates the use of a semiconductor chip that is connected via a number of signal leads (21-33) near the top surface of the semiconductor (see, *e.g.*, Figure 1; page 2, lines 109-111 of Schaper). Further, Schaper teaches that the disclosed capacitor element (20) has a planar ground member as its upper most conductive plate (see, *e.g.*, page 2, lines 122-124 of Schaper). The referenced patent discloses a standard high-speed very large scale integrated (VLSI) circuit, where the bottom side of the chip (14) is bonded to a plate (16) by a layer (18) of conductive epoxy cement (see, *e.g.*, page 2, lines 96-106 of Schaper). Additionally, Schaper teaches that the plate (16) to which the chip is mounted serves as a heat sink for the assembly. It is clear from this example that Schaper does not contemplate the use of flip-chip technology. As Schaper only contemplates ways to distribute power to and from an active side of a semiconductor die that faces away from the substrate, and additionally teaches that the bottom side of the plate is bonded to the plate by a layer of epoxy cement, Schaper actually teaches away from the use of a semiconductor die having an active side that faces the substrate. Applicant notes that a prior art reference that "teaches away" from the claimed invention is a *significant* factor to be considered in determining obviousness. *See In re Gurley*, 27 F.3d 551, 554 (Fed. Cir. 1994) (emphasis added).

The Examiner stated in the Office Action of August 25, 2004 that it would have

been obvious to modify the semiconductor device in Applicant's Prior Art to include a unitary capacitor as disclosed in Schaper. However, Applicant notes that the teaching or suggestion to make the claimed combination and the reasonable expectation of success must *both* be found in the prior art, *not* in Applicant's disclosure. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990) (emphasis added). *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (emphasis added). As acknowledged by the Examiner, Applicant's Prior Art does not teach the use of a windowframe capacitor. Additionally, Schaper is **completely silent** with regard to the use of flip-chip technology. Flip-Chip technology has existed for a number of years prior to the present invention. Thus, one skilled in the art would not look to Schaper, which discusses non-flip-chip technology, in light of Applicant's Prior Art, which discloses flip-chip technology. One skilled in the art would have no motivation based on the teachings of Schaper (or other prior art) to modify the semiconductor device of Applicant's Prior Art to include a unitary capacitor. Thus, without the present application as a guide, one skilled in the art would find no motivation or suggestion in Schaper to modify Applicant's Prior Art as discussed in the present application to arrive at the limitations of the claimed invention. See *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (emphasis added).

In view of the above, Applicant's Prior Art and Schaper are (i) not properly combinable and (ii) whether considered separately or in combination, fail to show or suggest the present invention as recited in independent claims 1 and 8 of the present application. Thus, independent claims 1 and 8 are patentable over Applicant's Prior Art and Schaper. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Claim 4

Claim 4 was rejected under 35 U.S.C. § 103 as being unpatentable over Applicant's Prior Art in view of United States Patent Application No. 2002/0011354 A1 in the Name of Barnett *et al.* (hereinafter "Barnett"). For the reasons set forth below, this rejection is respectfully traversed.

Like the above cited references, Barnett fails to disclose all the limitations of independent claim 1 of the present application or supply that which the above references lack. Barnett discloses a multichip module; that is, a chip carrier on which various chips are located that includes a carrier module with at least one cavity formed therein. The multichip module within the cavity has a submodule assembly that may be removed from the cavity (see paragraphs [0002] and [0004] of Barnett). Barnett does not show or suggest the use of a semiconductor die that has an active side that faces a substrate and the use of a unitary capacitor having an aperture in which the semiconductor die is disposed.

Therefore, like APA and Schaper, Barnett fails to disclose or otherwise teach the present invention as recited in independent claim 1 of the present application. Accordingly, because independent claim 1 has been shown to be patentable, claim 4 is allowable for at least the same reasons.

The Applicant further notes that there is no motivation to combine the teachings of APA with Schaper and Barnett. The Examiner cannot combine prior art references to render a claimed invention obvious by merely showing that all the limitations of the claimed invention can be found in the prior art references. Instead, there must be a suggestion or motivation to combine the references within the prior art references

themselves (MPEP § 2143). Regardless of whether prior art references can be combined, there must be an indication within the prior art references *expressing desirability* to combine the references to establish obviousness. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990); MPEP § 2143 (emphasis added). Further, the present application *cannot be used as a guide* in reconstructing elements of prior art references to render the claimed invention obvious. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must *both* be found in the prior art." *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991); MPEP § 2143 (emphasis added).

Moreover, the application of these three unrelated and non-combinable references is improper hindsight reconstruction of the claimed invention. Without the present application as a guide, one skilled in the art would not "pick and choose" features from three different references to achieve the claimed invention. In view of the lack of any teaching that would lead one skilled in the art to combine all of these references, such a combination could only be made based on the Applicant's own disclosure and is impermissible. *In re McLaughlin*, 443 F.2d 1392, 1395 (CCPA 1971); MPEP § 2145. Accordingly, the above references are not properly combinable in a rejection against the present application.

Claim 6

Claim 6 was rejected under 35 U.S.C. § 103 as being unpatentable over Applicant's Prior Art in view of Schaper and United States Patent No. 6,215,171 issued to Pape (hereinafter "Pape"). For the reasons set forth below, this rejection is respectfully traversed.

Like the above cited references, Pape fails to disclose all the limitations of

independent claim 1 of the present application or supply that which the above references lack. Pape discloses an integrated circuit (IC) module having additional electronic components (*e.g.*, capacitors) on a base inside the package of the IC module. The IC module was designed to facilitate operations at high operating frequencies (see col. 1, lines 28-63 of Pape). Pape does not show or suggest the use of a semiconductor die that has an active side that faces a substrate and the use of a unitary capacitor having an aperture in which the semiconductor die is disposed.

Therefore, like APA and Schaper, Pape fails to disclose or otherwise teach the present invention as recited in independent claim 1 of the present application. Accordingly, because independent claim 1 has been shown to be patentable, claim 6 is allowable for at least the same reasons.

Claim 9

Claim 9 was rejected under 35 U.S.C. § 103 as being unpatentable over Applicant's Prior Art in view of Schaper and United States Patent Application No. 2002/0011662 A1 in the Name of Komiya *et al.* (hereinafter "Komiya"). For the reasons set forth below, this rejection is respectfully traversed.

Like the above cited references, Komiya fails to disclose all the limitations of independent claim 8 of the present application or supply that which the above references lack. Komiya discloses a packaging substrate that includes a power supply layer and a semiconductor device that uses existing capacitance to reduce power supply impedance (see paragraph [0006] of Komiya). Komiya does not show or suggest the use of a unitary capacitor.

Therefore, like APA and Schaper, Komiya fails to disclose or otherwise teach the

present invention as recited in independent claim 8 of the present application. Accordingly, because independent claim 8 has been shown to be patentable, claim 9 is allowable for at least the same reasons.

Claim 10

Claim 10 was rejected under 35 U.S.C. § 103 as being unpatentable over Applicant's Prior Art in view of Schaper and United States Patent No. 4,827,323 issued to Tigelaar *et al.* (hereinafter "Tigelaar"). For the reasons set forth below, this rejection is respectfully traversed.

Like the above cited references, Tigelaar fails to disclose all the limitations of independent claim 8 of the present application or supply that which the above references lack. Tigelaar discloses a structure for increased capacitance that occupies a minimum of surface area on an integrated circuit. Tigelaar discloses a capacitor stack that includes interleaved capacitor plates that are separated by a dielectric material (see col. 1 lines 31-57 of Tigelaar). Tigelaar is completely silent with respect to the use of a semiconductor die that has an active side that faces a substrate and the use of a unitary capacitor having an aperture in which the semiconductor die is disposed.

Therefore, like APA and Schaper, Tigelaar fails to disclose or otherwise teach the present invention as recited independent claim 8 of the present application. Accordingly, because independent claim 8 has been shown to be patentable, claim 10 is allowable for at least the same reasons.

Claims 12-14

Claims 12-14 were rejected under 35 U.S.C. § 103 as being unpatentable over Applicant's Prior Art in view of Schaper and United States Patent No. 4,839,712 issued

to Mamodaly *et al.* (hereinafter "Mamodaly"). For the reasons set forth below, this rejection is respectfully traversed.

Like the above cited references, Mamodaly fails to disclose all the limitations of independent claim 8 of the present application or supply that which the above references lack. Mamodaly discloses a compact combiner for ultra-high frequency devices (see abstract of Mamodaly). As shown in Figure 6 of Mamodaly, a semiconductor **1** is fixed to a metal base **11**. Additionally, a number of capacitors **5** are placed around the semiconductor **1** (see col. 6, lines 45-56 of Mamodaly). Mamodaly is completely silent with respect to the use of a semiconductor die that has an active side that faces a substrate and the use of a unitary capacitor having an aperture in which the semiconductor die is disposed.

Therefore, like APA and Schaper, Mamodaly fails to disclose or otherwise teach the present invention as recited in independent claim 8 of the present application. Accordingly, because independent claim 8 has been shown to be patentable, claims 12-14 are allowable for at least the same reasons.

Claim 15

Claim 15 was rejected under 35 U.S.C. § 103 as being unpatentable over Applicant's Prior Art in view of Schaper, Mamodaly, and Barnett. For the reasons set forth below, this rejection is respectfully traversed.

As discussed above, Schaper and Mamodaly fail to disclose all the limitations of independent claim 8 of the present application. Additionally, as discussed above, Barnett fails to show or suggest the use of a semiconductor die that has an active side that faces a substrate and the use of a unitary capacitor having an aperture in which the

semiconductor die is disposed.

Therefore, APA, Schaper, Mamodaly and Barnett, whether taken separately or in any combination, fail to disclose or otherwise teach the present invention as recited in independent claim 8 of the present application. Accordingly, because independent claim 8 has been shown to be patentable, claims 12-14 are allowable for at least the same reasons.

The Applicant further notes that there is no motivation to combine the teachings of APA with Schaper, Mamodaly, and Barnett. The Examiner cannot combine prior art references to render a claimed invention obvious by merely showing that all the limitations of the claimed invention can be found in the prior art references. Instead, there must be a suggestion or motivation to combine the references within the prior art references themselves (MPEP § 2143). Regardless of whether prior art references can be combined, there must be an indication within the prior art references *expressing desirability* to combine the references to establish obviousness. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990); MPEP § 2143 (emphasis added). Further, the present application *cannot be used as a guide* in reconstructing elements of prior art references to render the claimed invention obvious. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must *both* be found in the prior art." *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991); MPEP § 2143 (emphasis added).

Moreover, the application of these **four** unrelated and non-combinable references is improper hindsight reconstruction of the claimed invention. Without the present application as a guide, one skilled in the art would not "pick and choose" features from **four** different references to achieve the claimed invention. In view of the lack of any

teaching that would lead one skilled in the art to combine all of these references, such a combination could only be made based on the Applicant's own disclosure and is impermissible. *In re McLaughlin*, 443 F.2d 1392, 1395 (CCPA 1971); MPEP § 2145. Accordingly, the above references are not properly combinable in a rejection against the present application.

Claim 16

Claim 16 was rejected under 35 U.S.C. § 103 as being unpatentable over Applicant's Prior Art in view of Schaper, Mamodaly, Barnett, and Pape. For the reasons set forth below, this rejection is respectfully traversed.

As discussed above, APA, Schaper, and Mamodaly fail to disclose all the limitations of independent claim 8 of the present application. Further, as discussed above, Barnett and Pape fail to disclose the use of a semiconductor die that has an active side that faces a substrate or the use of a unitary capacitor. Thus, each of the cited references fails to show or suggest the use of a semiconductor die that has an active side that faces a substrate and the use of a unitary capacitor having an aperture in which the semiconductor die is disposed.

Therefore, APA, Schaper, Mamodaly, Barnett, and Pape, whether taken separately or in any combination, fail to disclose or otherwise teach the present invention as recited in independent claim 8 of the present application. Accordingly, because independent claim 8 has been shown to be patentable, claims 12-14 are allowable for at least the same reasons.

The Applicant further notes that there is no motivation to combine the teachings of APA with Schaper, Mamodaly, and Barnett and Pape. The Examiner cannot combine

prior art references to render a claimed invention obvious by merely showing that all the limitations of the claimed invention can be found in the prior art references. Instead, there must be a suggestion or motivation to combine the references within the prior art references themselves (MPEP § 2143). Regardless of whether prior art references can be combined, there must be an indication within the prior art references *expressing desirability* to combine the references to establish obviousness. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990); MPEP § 2143 (emphasis added). Further, the present application *cannot be used as a guide* in reconstructing elements of prior art references to render the claimed invention obvious. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must *both* be found in the prior art." *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991); MPEP § 2143 (emphasis added).

Moreover, the application of these **five** unrelated and non-combinable references is improper hindsight reconstruction of the claimed invention. Without the present application as a guide, one skilled in the art would not "pick and choose" features from **five** different references to achieve the claimed invention. In view of the lack of any teaching that would lead one skilled in the art to combine all of these references, such a combination could only be made based on the Applicant's own disclosure and is impermissible. *In re McLaughlin*, 443 F.2d 1392, 1395 (CCPA 1971); MPEP § 2145. Accordingly, the above references are not properly combinable in a rejection against the present application.

Conclusion

The above remarks are believed to require no further prior art search. Also, Applicant believes that this reply is responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.092001; P5787).

Respectfully submitted,

Date: 11/24/04

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